Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) Apparatus, comprising:

a digital data channel which stores input data to a data storage medium and subsequently retrieves output data from the medium ~~corresponding to~~ made from the input data; and

~~an emulation~~ a circuit~~,~~ connected to the digital data channel~~,~~ which can characterize the input and output data in at least two alternative digital configurations and predict error rate performance in relation to each configuration ~~arranges the input data into an input sequence of multibit symbols each having a first selected symbol length and arranges the output data into an output sequence of multibit symbols each having the first selected symbol length, wherein the emulation circuit determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence to predict error rate performance of the digital data channel~~.

2. (Currently amended) The Apparatus of claim 1, wherein the input data is characterized as an input sequence of multibit symbols each having a first selected symbol length and the output data is characterized as an output sequence of multibit symbols each having the first selected symbol length ~~emulation circuit comprises a memory having a first memory location and a second memory location, wherein the input data are stored in the first memory location and the output data are stored in the second memory location~~.

3. (Currently amended) The Apparatus of claim 2 ~~1, wherein the input sequence is characterized as a first input sequence, the output sequence is characterized as a first output sequence,~~ wherein the ~~emulation~~ circuit ~~further operates to arrange~~ characterizes the input data into a second input sequence of multibit symbols each having a second selected symbol length different from the first selected symbol length and operates to arrange the output data into a second output sequence of multibit symbols each having the second selected symbol length~~, and wherein the emulation circuit further operates to determine a number of erroneous symbols in the second output sequence in relation to differences between the second input sequence and the second output sequence to predict error rate performance of the digital data channel~~.

4. (Currently amended) The apparatus of claim 1, wherein the ~~emulation~~ circuit ~~comprises a field programmable gate array (FPGA)~~ predicts the error rate performance in relation to only one digital configuration of the input and output data.

5. (Currently amended) The apparatus of claim 1, wherein the ~~emulation~~ circuit performs run length limited (RLL) encoding upon the input data prior to ~~arrangement of~~ characterizing the input data ~~into the input sequence~~, and wherein the ~~emulation~~ circuit further inhibits RLL decoding of the output data ~~so that the output sequence is formed of bits that nominally~~ to reflect said RLL encoding.

6. (Currently amended) The apparatus of claim 1, wherein the ~~emulation~~ circuit determines the number of ~~erroneous symbols~~ errors in the output ~~sequence~~ data in relation to a ~~total~~ preselected number of ~~said symbols greater than a first selected number of erroneous symbols~~ errors that can be corrected by a first error correction code (ECC) encoding methodology.

7. (Currently amended) The apparatus of claim 1, wherein the ~~emulation~~ circuit arranges the ~~symbols of~~ the input ~~sequence~~ data into a plurality of interleaves and arranges the ~~symbols of the~~ output ~~sequence~~ data into a corresponding plurality of interleaves.

8. (Currently amended) The apparatus of claim 1, wherein the ~~digital data channel comprises a digital circuit and wherein the emulation~~ circuit concurrently inhibits and emulates selected operation of the digital ~~circuit~~ data channel.

9. (Currently amended) The apparatus of claim ~~8, wherein the digital circuit comprises an interface controller comprising a programmable microprocessor~~ 2 wherein the circuit determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence.

10. (Currently amended) The apparatus of claim ~~8, wherein the digital circuit comprises a run length limited (RLL) decoder~~ 3 wherein the circuit determines a number of erroneous symbols in the second output sequence in relation to differences between the second input sequence and the second output sequence.

11. (Currently amended) The apparatus of claim ~~8, wherein the digital circuit comprises a Viterbi detector~~ 1 wherein the circuit predicts the error rate performance in relation to two or more digital configurations of the input and output data.

12. (Currently amended) The apparatus of claim ~~1,~~ 2 wherein the ~~emulation~~ circuit comprises a symbol comparator circuit comprising a plurality of state machines each configured to arrange a selected set of data into a selected number of different symbol lengths ~~including the first selected symbol length~~.

13. (Currently amended) The apparatus of claim 12, wherein the symbols of the input sequence and the output sequence are respectively arranged into corresponding pluralities of interleaves, and wherein the ~~emulation~~ circuit further comprises an interleave counter circuit which determines an uncorrectable number of erroneous symbols in each interleave that exceed a correctable number of erroneous symbols that can be detected by a first ECC encoding methodology.

14. (Currently amended)) The apparatus of claim 13, wherein the ~~emulation~~ circuit further comprises a counter which ~~accumulates the first number in relation to~~ indicates the respective uncorrectable numbers determined by the interleave counter circuit for each respective interleave.

15. (Currently amended) Method, comprising:

using a digital data channel to store input data to a data storage medium~~, said input data comprising an input stream of data bits~~;

subsequently using the digital data channel to obtain output data from the medium~~, said output data comprising an output stream of data bits corresponding to the input stream of data bits~~;

arranging the input data into ~~an input sequence of multibit symbols, each symbol having a first selected symbol length~~ a selected digital configuration from a plurality of different selectable digital configurations;

arranging the output data into ~~an output sequence of multibit symbols, each symbol having the first selected symbol length~~ the selected digital configuration; and

comparing the output ~~sequence~~ data with the input ~~sequence~~ data to determine ~~a first number of erroneous symbols in the output sequence~~ an error rate performance.

16. (Currently amended) The method of claim 15~~, further comprising: predicting error rate performance of the digital data channel~~ wherein the comparing step is characterized by using a first error correction code (ECC) encoding methodology based on the ~~first selected symbol length~~ selected digital configuration.

17. (Currently amended) The method of claim 16, wherein the comparing step ~~comprises~~ is characterized by determining ~~the first~~ a number of ~~erroneous symbols~~ errors in the output ~~sequence~~ data in relation to a selected number of ~~erroneous symbols~~ errors that can be detected by the first error correction code (ECC) encoding methodology.

18. (Currently amended) The method of claim 15, ~~further comprising: providing a memory having a first memory location and a second memory location; storing the input data in the first memory location; and storing the output data in the second memory location~~ wherein the arranging the input and output data steps are characterized by sequences of multibit symbols each having a selected symbol length.

19. (Currently amended) The method of claim ~~15, wherein the input sequence is characterized as a first input sequence and the output sequence is characterized as a first output sequence, and wherein the method further comprises: further arranging the input data into a second input sequence of multibit symbols, each symbol having a second selected symbol length different from the first selected symbol length; further arranging the output data into a second output sequence of multibit symbols, each symbol having the second selected symbol length; and comparing the second output sequence with the second input sequence to determine a second number of erroneous symbols in the second output sequence~~ wherein the arranging the input and output data steps are characterized by sequences of multibit symbols each having a second selected symbol length.

20. (Currently amended) The method of claim 19~~, further comprising:~~ wherein the comparing step is characterized by predicting error rate performance ~~of the digital data channel~~ using a second error correction code (ECC) encoding methodology based on the second selected symbol length.

21. (Currently amended) The method of claim 15~~, further comprising:~~ wherein the arranging the input and output data steps are characterized by performing run length limited (RLL) encoding upon the input data ~~prior to arrangement of the input data into the input sequence and storage of the input data to the medium;~~ and inhibiting RLL decoding of the output data ~~so that the output sequence is formed of bits that nominally~~ to reflect said RLL encoding.

22. (Currently amended) The method of claim 15, wherein the arranging the input and output data ~~step comprises~~ steps are characterized by arranging the ~~multibit symbols of the input sequence~~ data into a plurality of interleaves~~, and wherein the arranging the output data step comprises arranging the multibit symbols of the output sequence into a corresponding plurality of interleaves~~.

23. (Currently amended) The method of claim 15~~, wherein the digital data channel comprises a digital circuit block, and wherein the method further comprises~~ comprising concurrently inhibiting and emulating selected operation of the digital ~~circuit block~~ data channel.

24. (Currently amended) The method of claim ~~23, wherein the digital circuit comprises an interface controller comprising a programmable microprocessor~~ 15 wherein the comparing step is characterized by predicting the error rate in relation to only one selected digital configuration of the input and output data.

25. (Currently amended) The method of claim ~~23, wherein the digital circuit comprises a run length limited (RLL) decoder~~ 15 wherein the comparing step is characterized by predicting the error rate in relation to two or more selected digital configurations of the input and output data.

26. (Currently amended) The method of claim ~~23, wherein the digital circuit comprises a Viterbi detector~~ 18 wherein the comparing step is characterized by predicting the error rate in relation to differences between the input sequence and the output sequence.

27. (Original) A disc drive comprising a digital data channel configured in accordance with the method of claim 15.